**FIG. 1**

proc ssing syst m 10

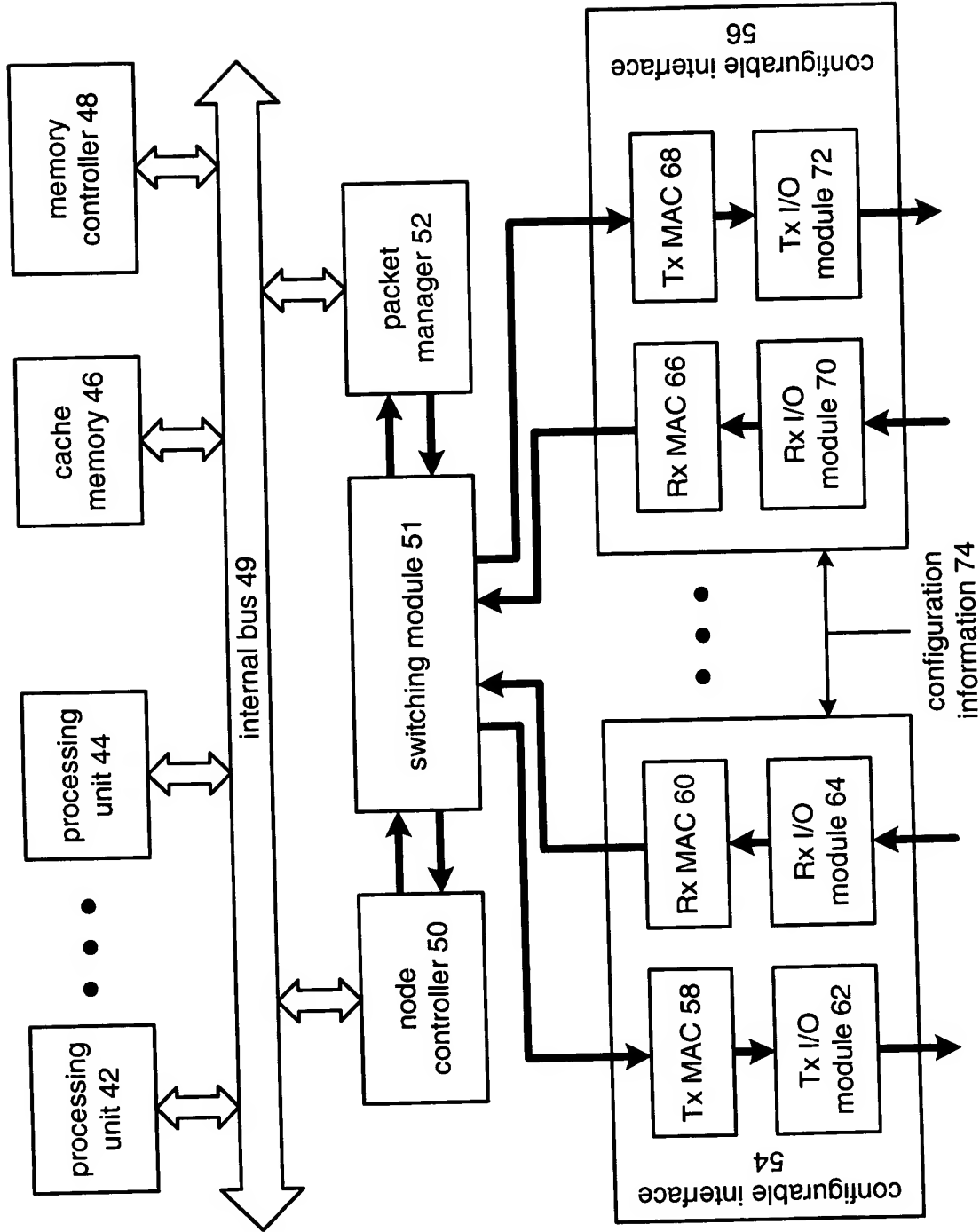


FIG. 2
processing device 20

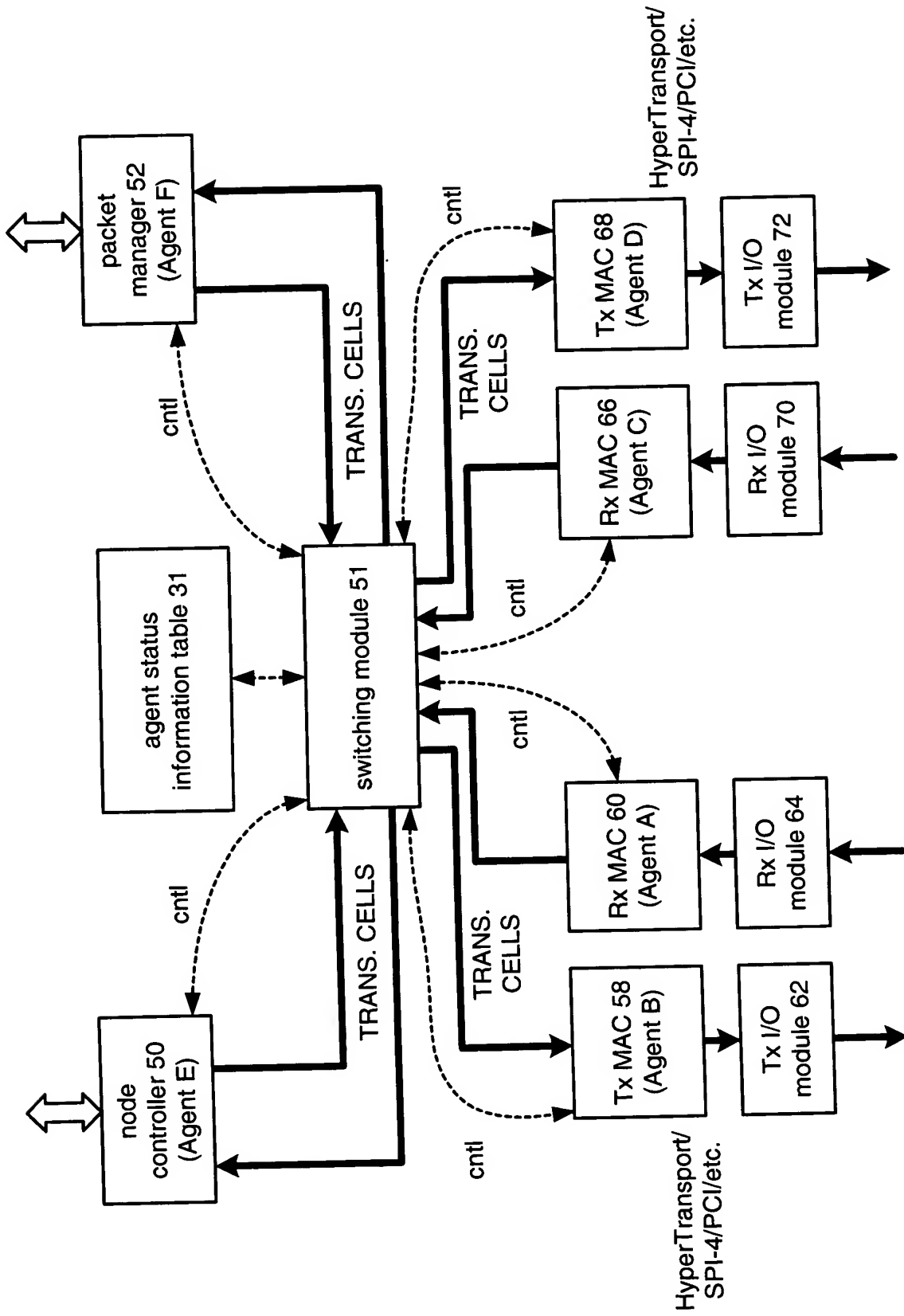


FIG. 3
processing device 20

CONTROL TAG (4 BYTES)	DATA (16 BYTES)
-----------------------------	--------------------

Transaction Cell

FIG. 4A

SRC_AGT_A STATUS	DST_AGT_B STATUS	EOP_ST
SRC_AGT_A STATUS	DST_AGT_D STATUS	EOP_ST
SRC_AGT_A STATUS	DST_AGT_E STATUS	EOP_ST
SRC_AGT_A STATUS	DST_AGT_F STATUS	EOP_ST
SRC_AGT_C STATUS	DST_AGT_B STATUS	EOP_ST
SRC_AGT_C STATUS	DST_AGT_D STATUS	EOP_ST
SRC_AGT_C STATUS	DST_AGT_E STATUS	EOP_ST
SRC_AGT_C STATUS	DST_AGT_F STATUS	EOP_ST
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
SRC_AGT_F STATUS	DST_AGT_B STATUS	EOP_ST
SRC_AGT_F STATUS	DST_AGT_D STATUS	EOP_ST
SRC_AGT_F STATUS	DST_AGT_E STATUS	EOP_ST

Agent Status Information Table

FIG. 4B

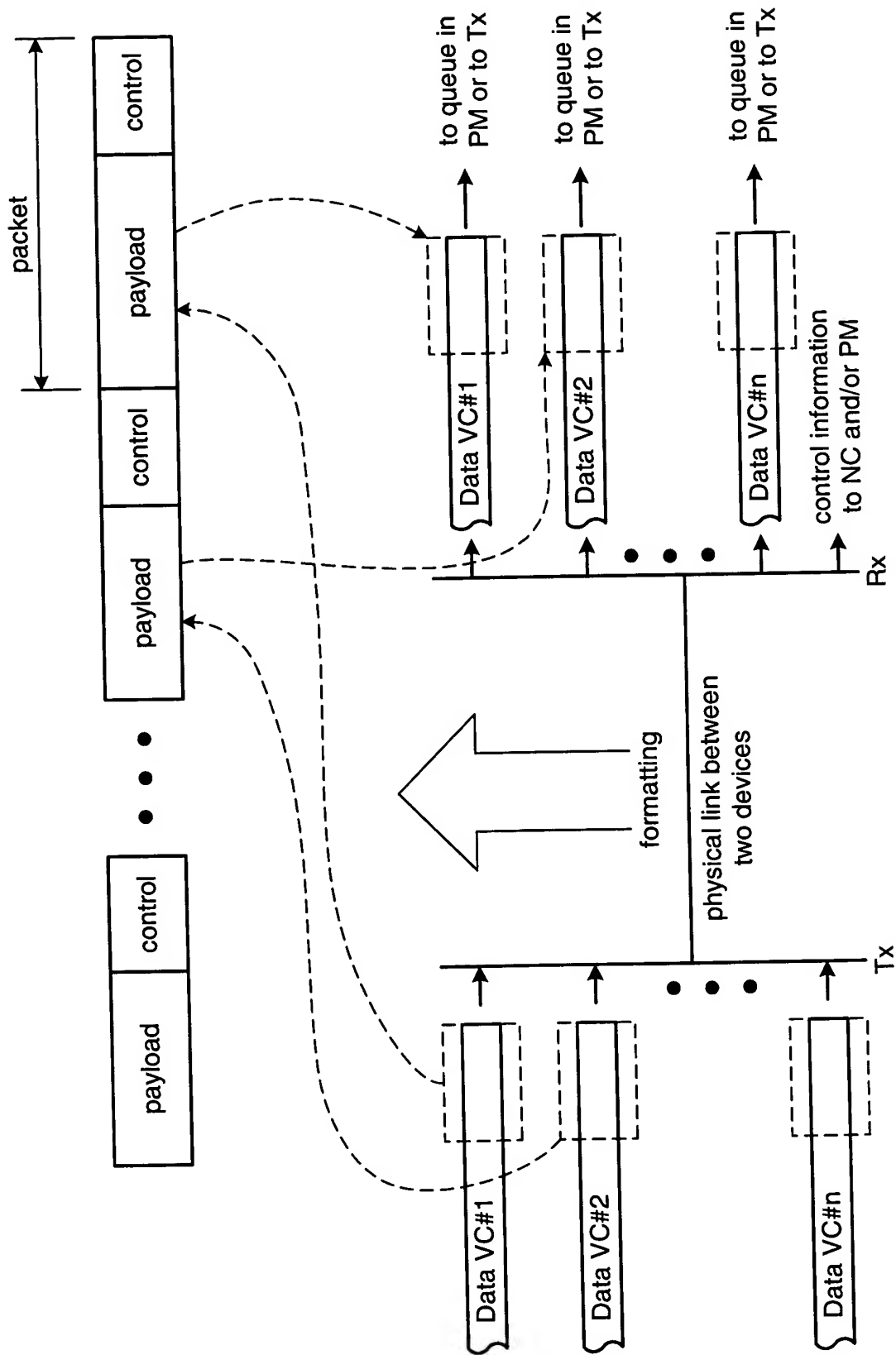


FIG. 5
data mapping for I/O modules 62,
64, 70, and/or 72

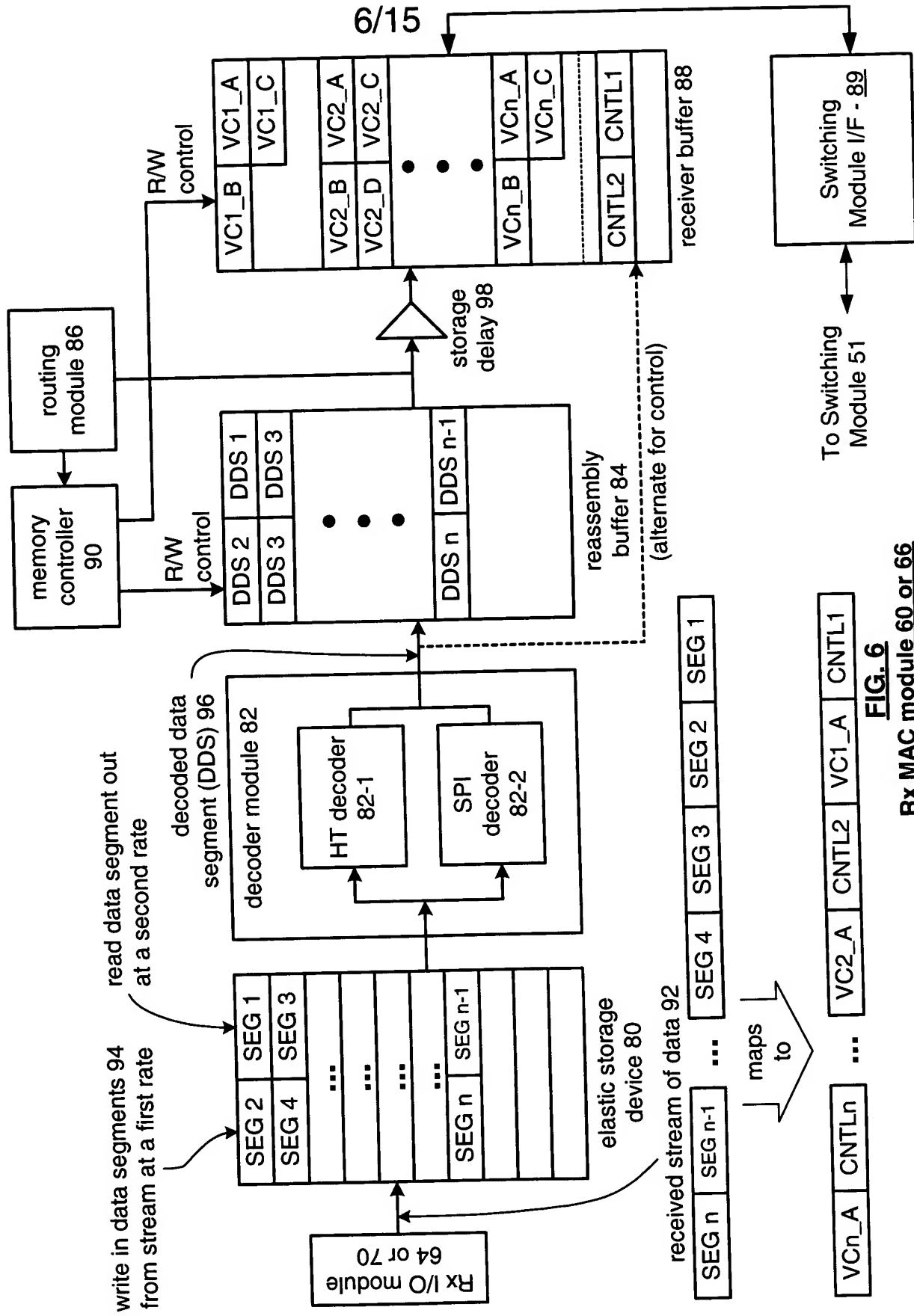


FIG. 6

Rx MAC module 60 or 66

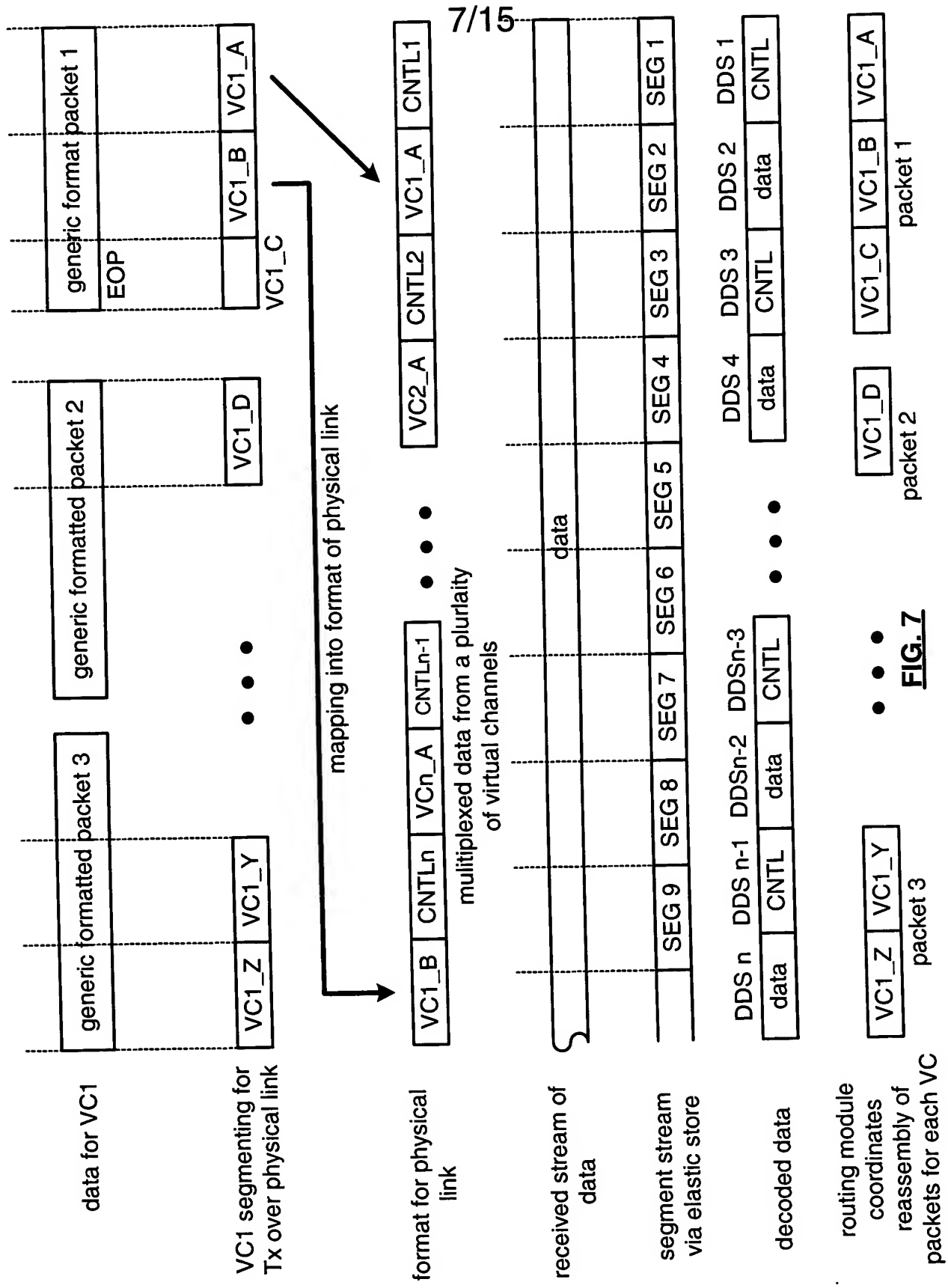


FIG. 7

OVC lists: 64 for packets, 4x4 for CCNUMA = 80 lists
IVC Lists: 16 for packets, 4 for CCNUMA = 20 lists
Free linked list - 1 list

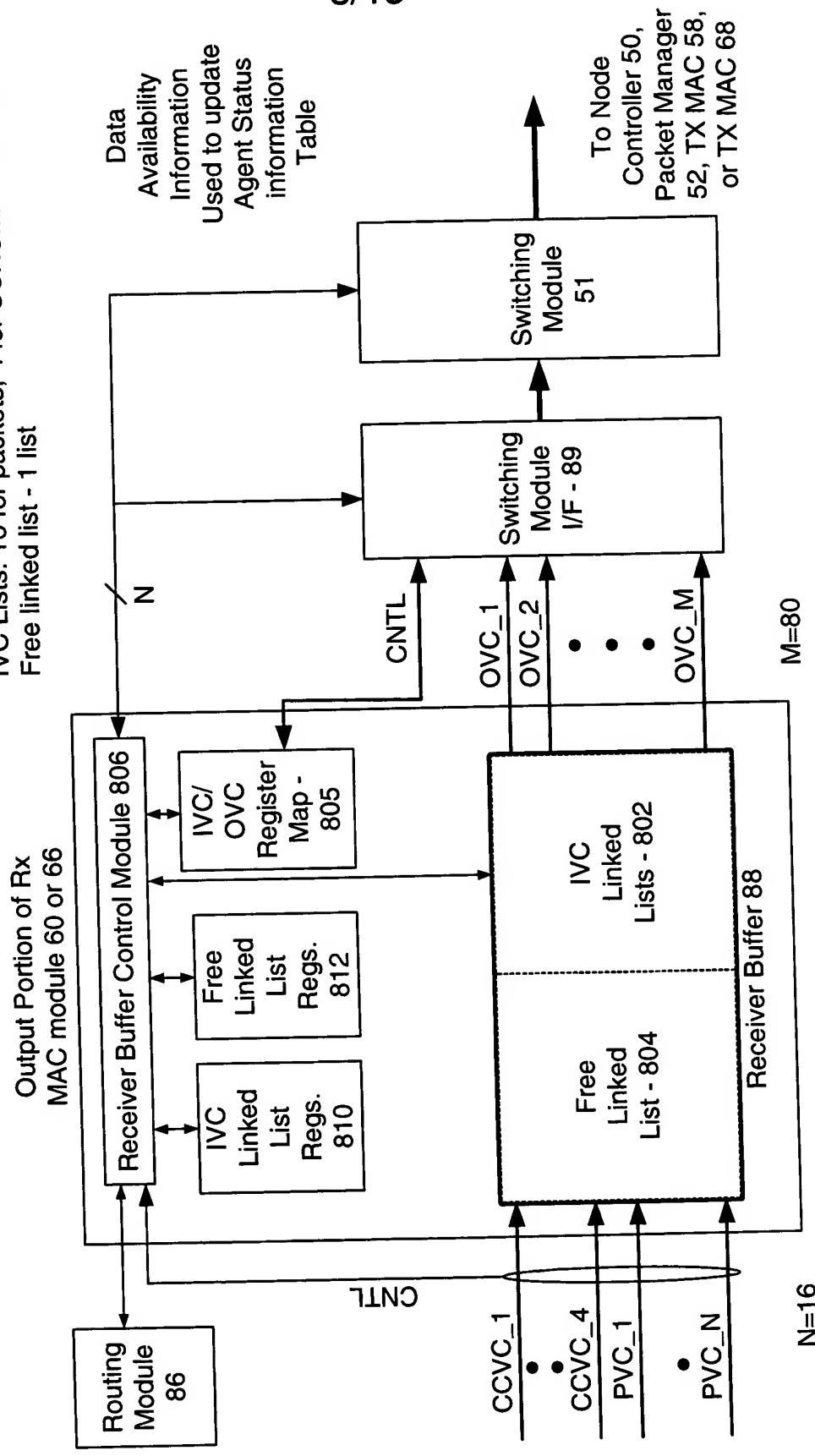


FIG. 8

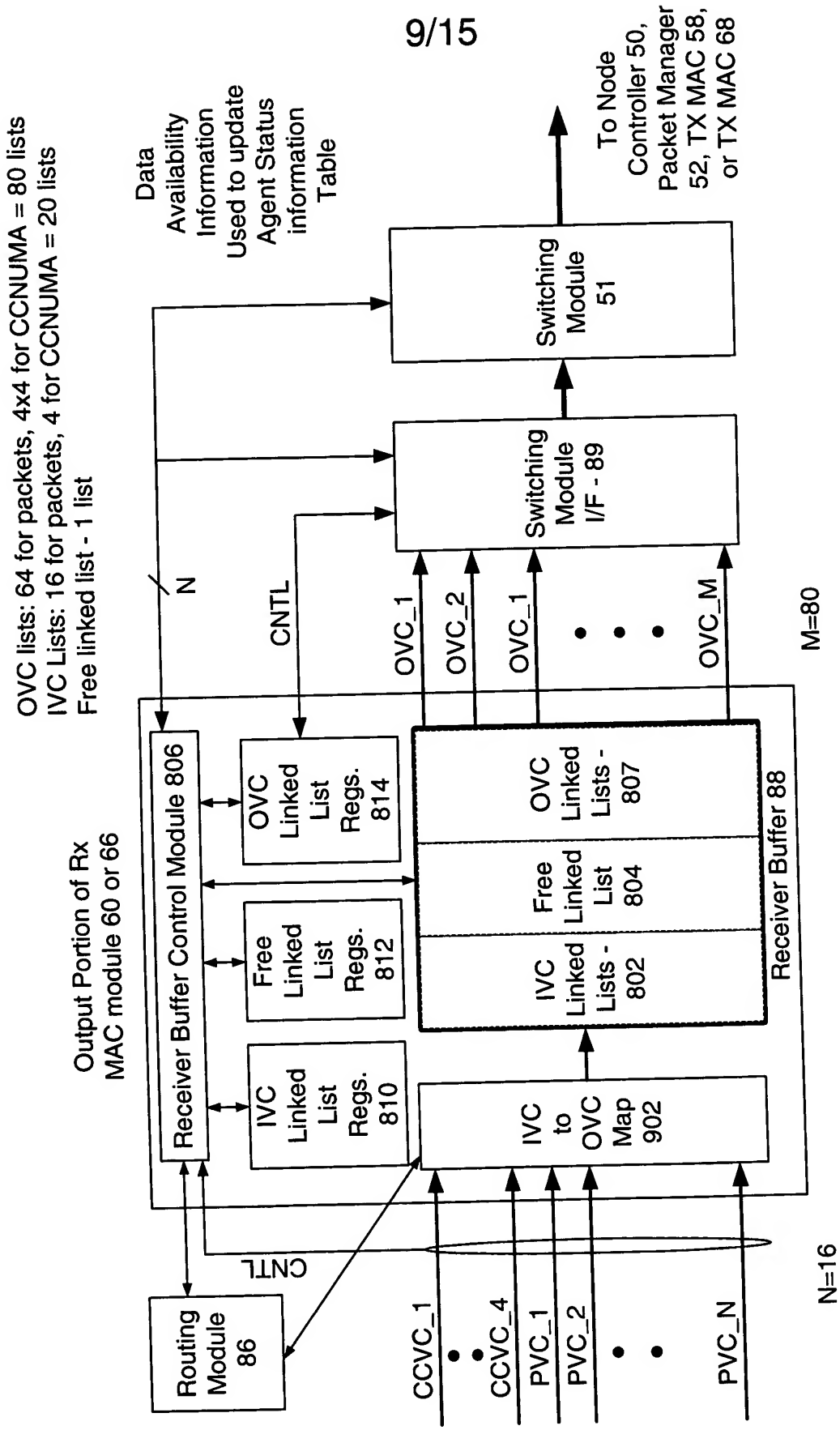


FIG. 9

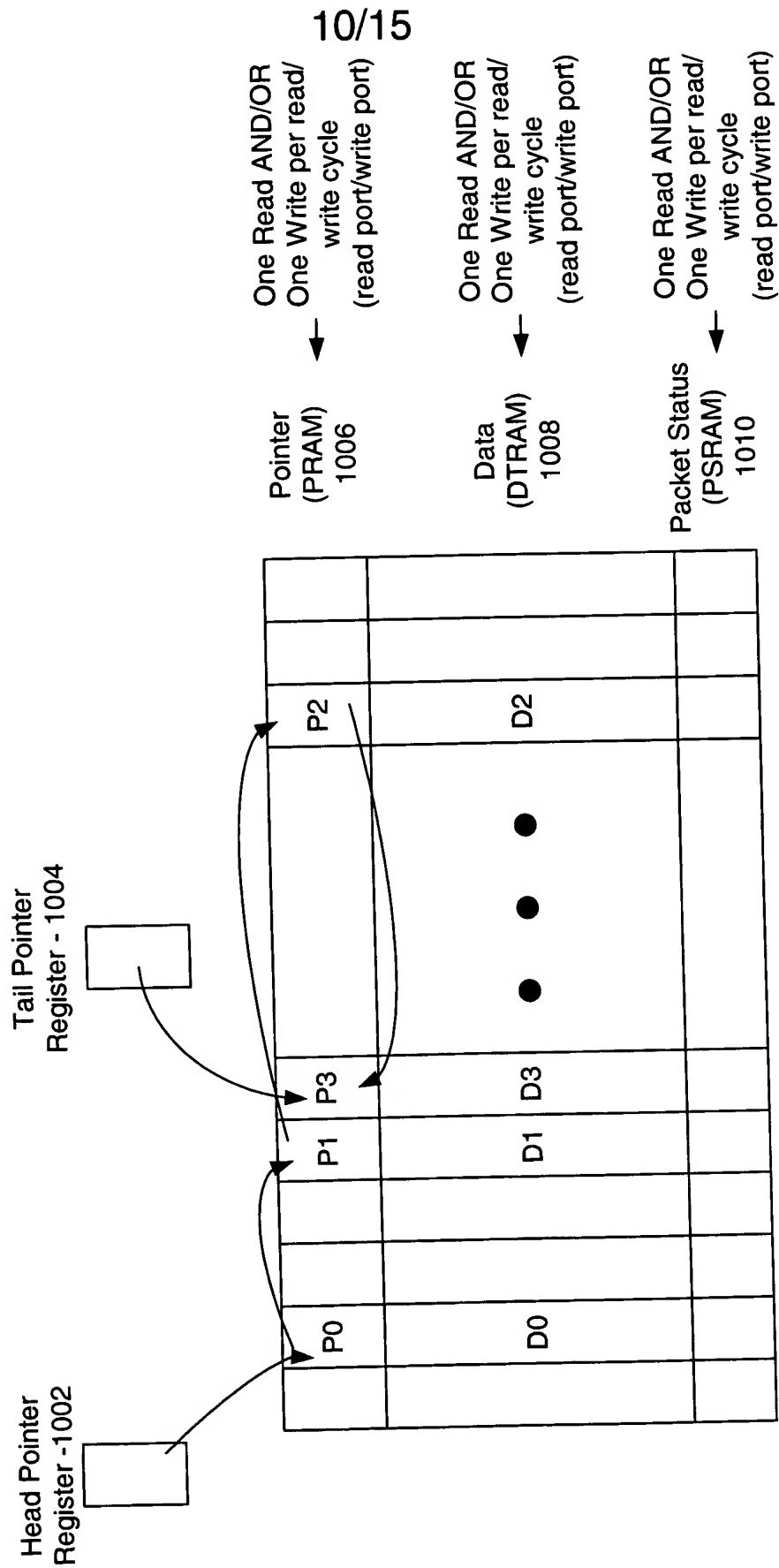


FIG. 10

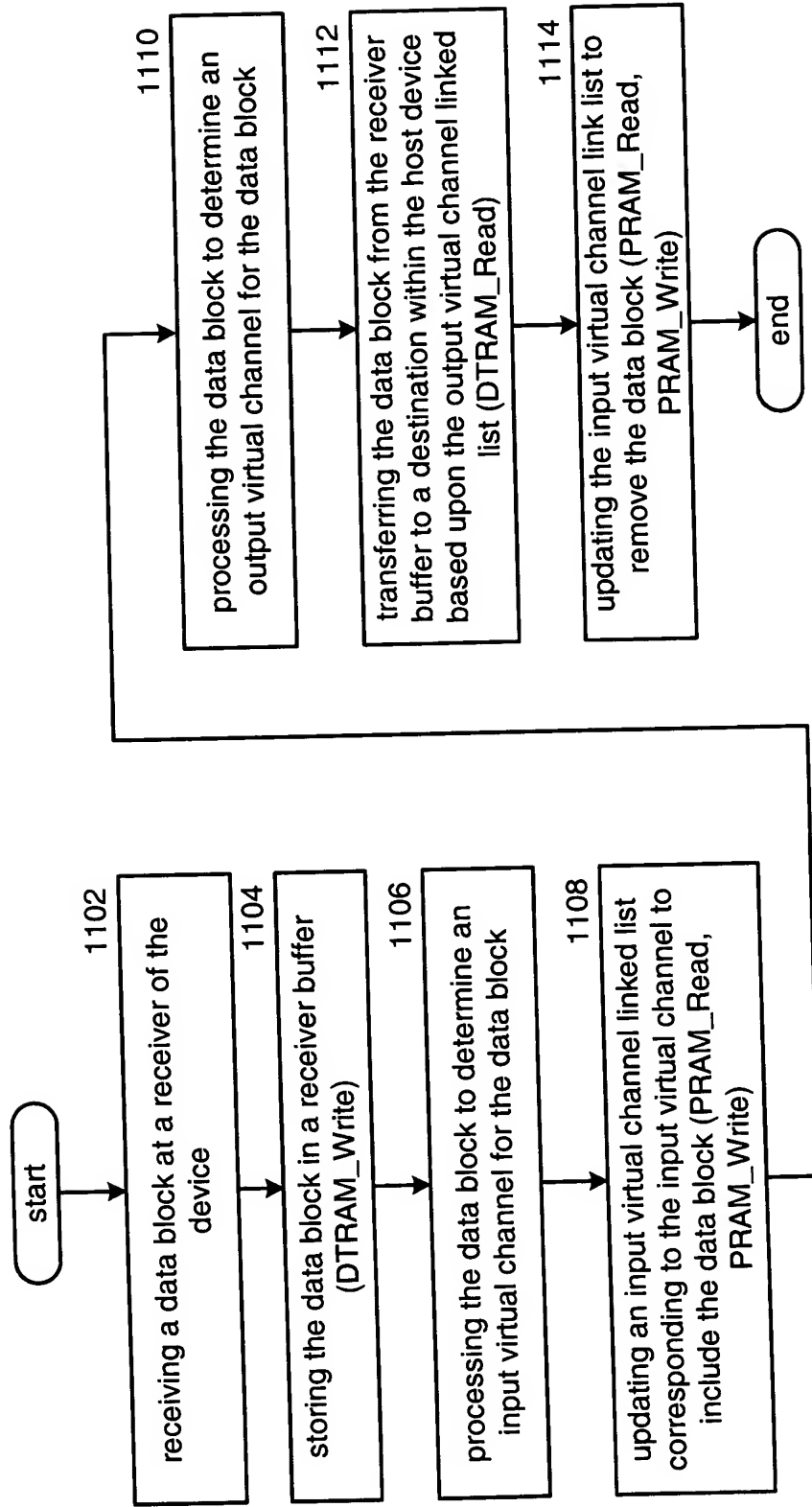
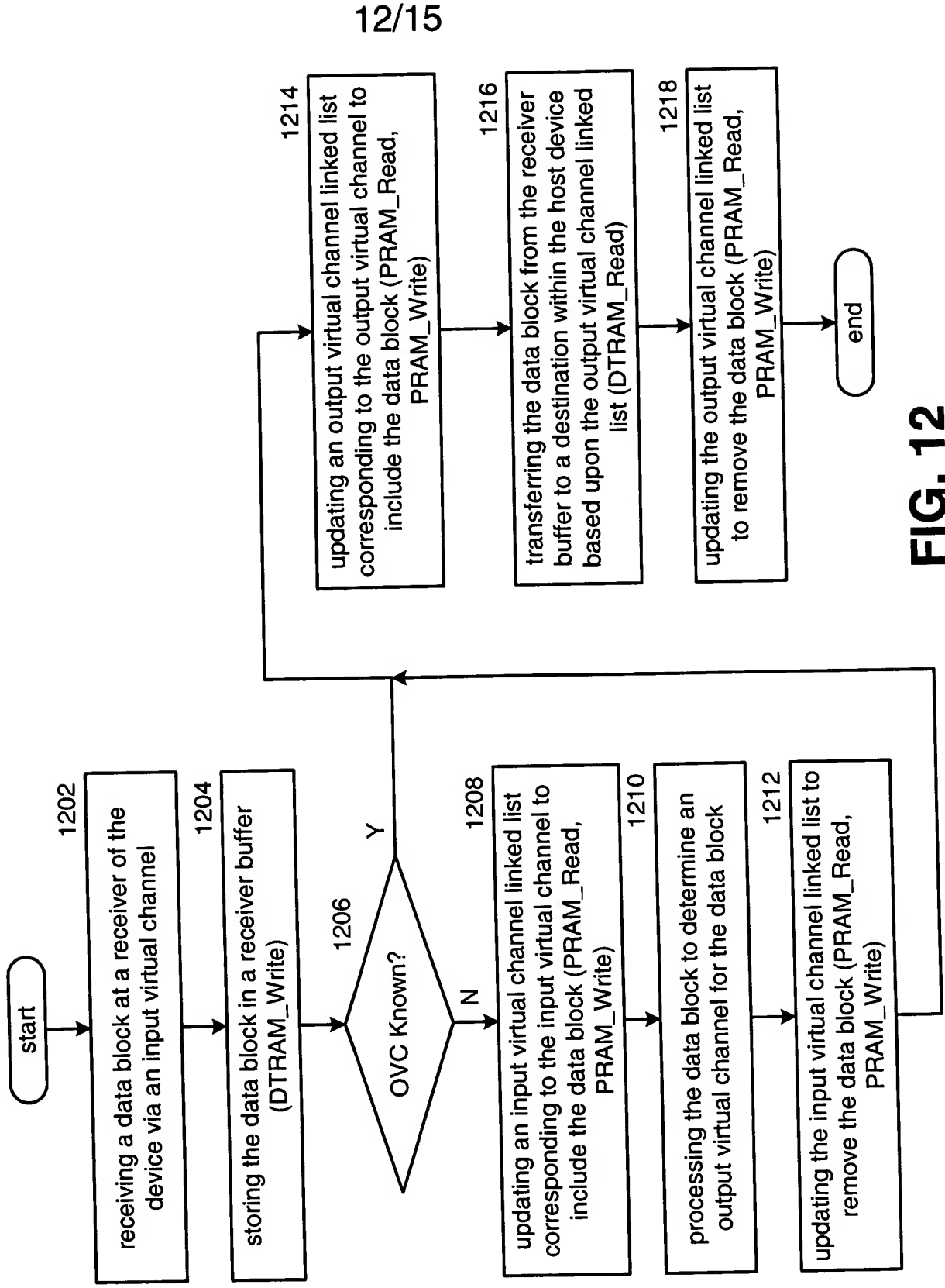


FIG. 11



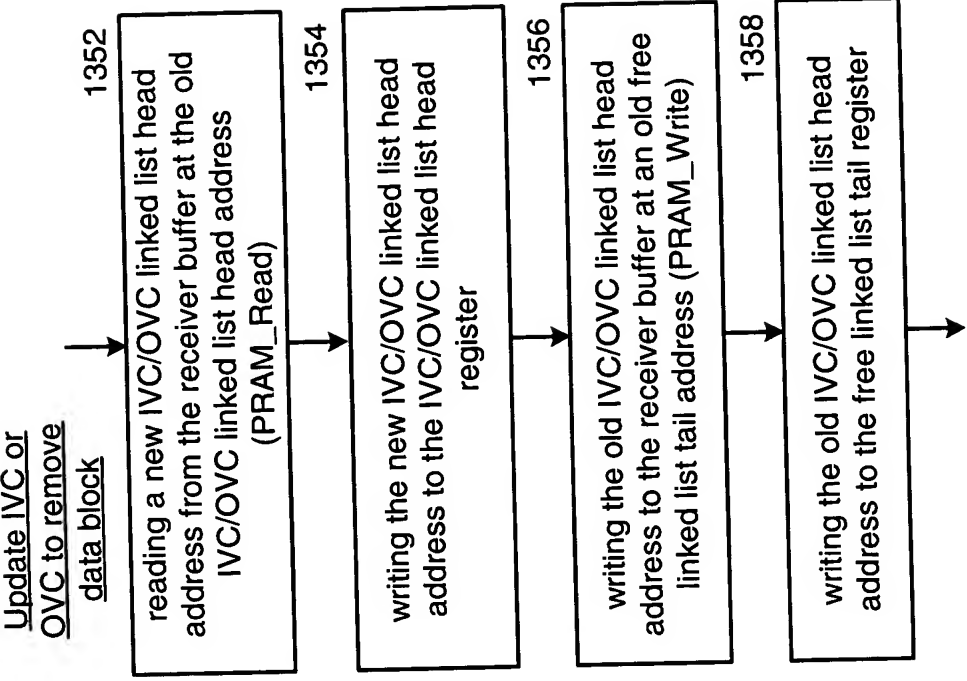


FIG. 13B

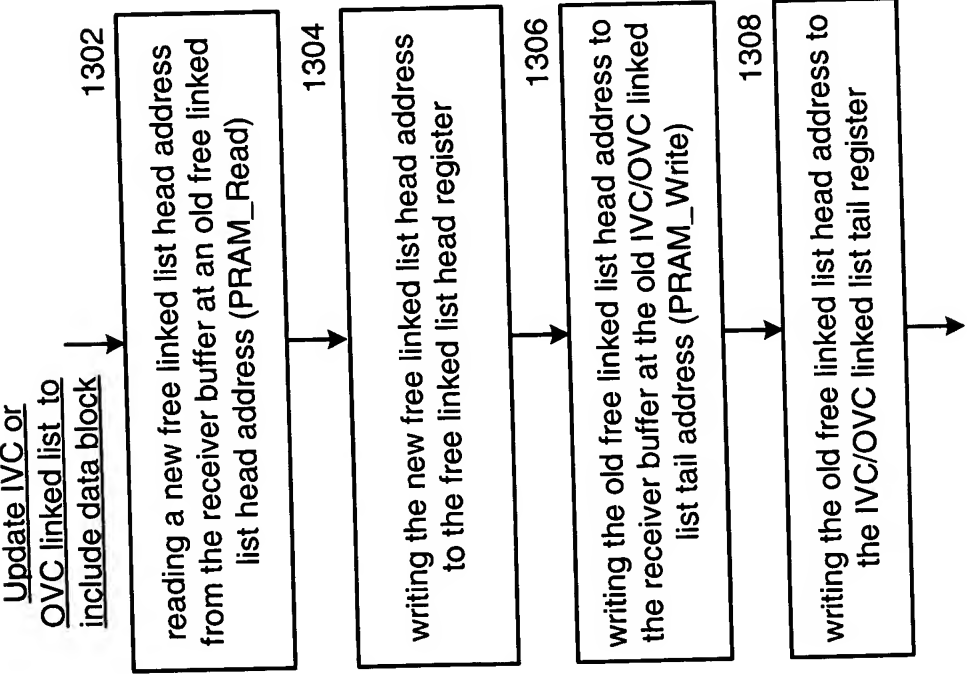


FIG. 13A

Read from
OVC and
Write to IVC
in a single
read/write
cycle

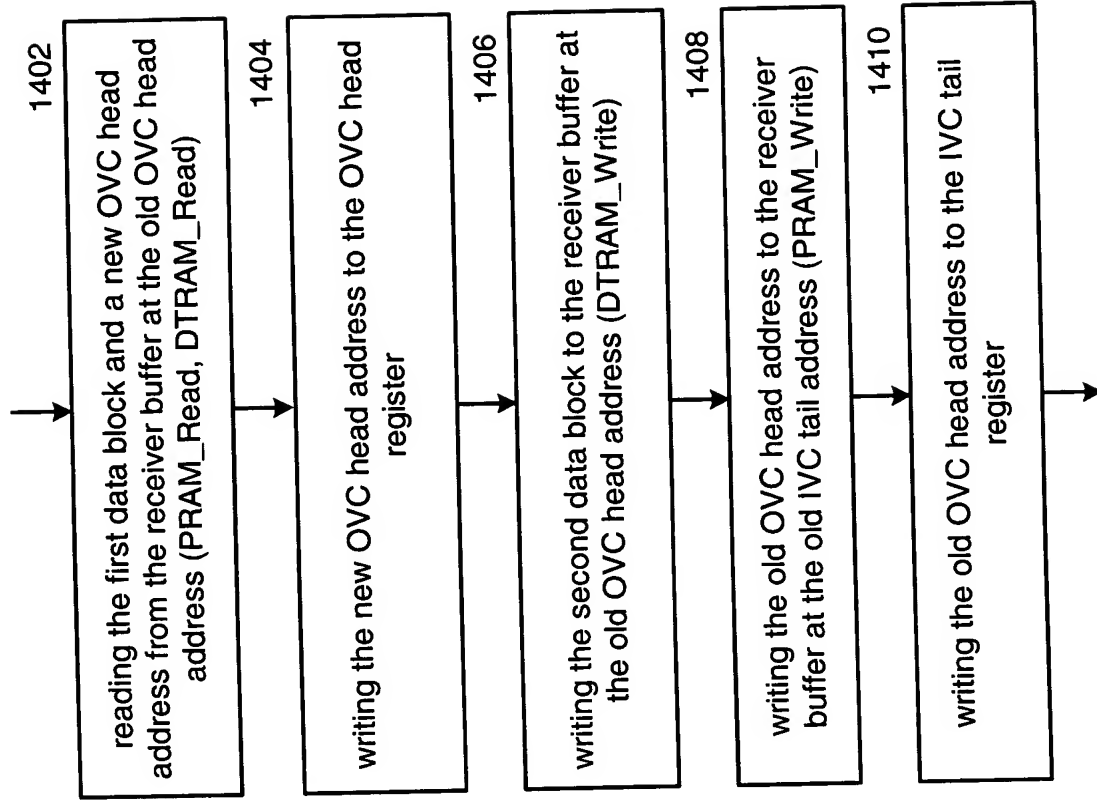


FIG. 14

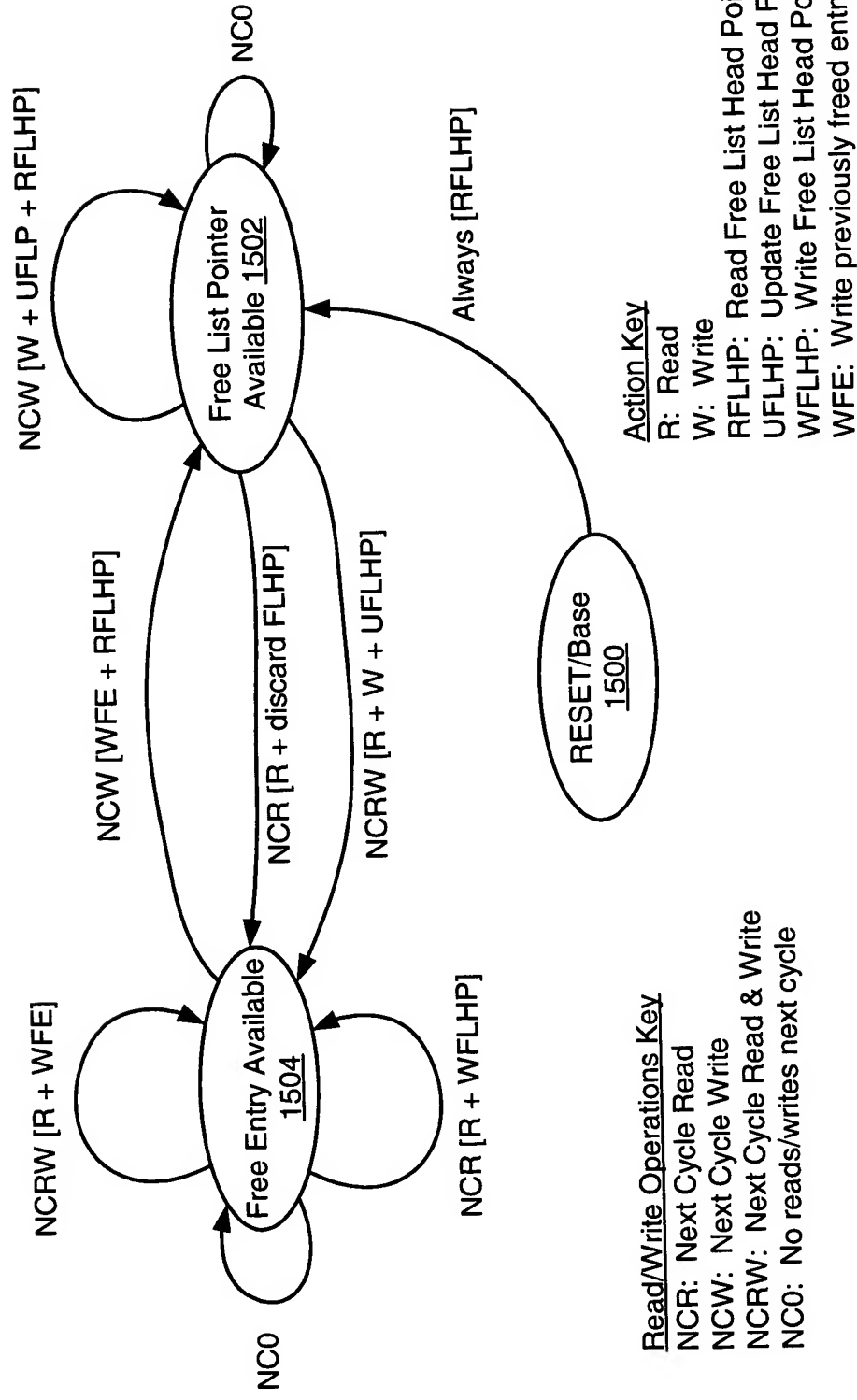


FIG. 15